

WHAT IS CLAIMED IS:

1 1. For use with an operational circuit comprising at least
2 one high-impedance node, a pull-down circuit capable of pulling
3 said high-impedance node down to ground when a pull-down (PD)
4 signal driving said pull-down circuit is Logic 1, said pull-down
5 circuit comprising:

6 a first pull-down N-channel transistor having a drain
7 coupled to said high-impedance node, a gate coupled to said PD
8 signal, and a source coupled to a common node;

9 a second pull-down N-channel transistor having a drain
10 coupled to said common node, a gate coupled to said PD signal, and
11 a source coupled to a ground rail;, wherein said first and second
12 pull-down N-channel transistors are off when said PD signal is
13 Logic 0 and are on when said PD signal is Logic 1; and

14 a gate-biasing circuit driven by said PD signal, wherein
15 said gate-biasing circuit is off when said PD signal is Logic 1 and
16 said gate-biasing circuit applies a Logic 1 bias voltage to said
17 common node when said PD signal is Logic 0, said Logic 1 bias
18 voltage creating a negative V_{gs} bias on said first pull-down N-
19 channel transistor when said PD signal is Logic 0.

1 2. The pull-down circuit as set forth in Claim 1 wherein
2 said gate-biasing circuit comprises a P-channel transistor having a
3 gate coupled to said PD signal, a drain coupled to said common
4 node, and a source coupled to a VDD power supply rail.

1 3. The pull-down circuit as set forth in Claim 2 wherein
2 said operational circuit is a phase-locked loop (PLL).

1 4. The pull-down circuit as set forth in Claim 1 wherein
2 said gate-biasing circuit comprises:

3 an inverter having an input coupled to said PD signal;
4 and

5 a biasing N-channel transistor having a gate coupled to
6 an output of said inverter, a source coupled to said common node,
7 and a drain coupled to a VDD power supply rail.

1 5. The pull-down circuit as set forth in Claim 4 wherein
2 said operational circuit is a phase-locked loop (PLL).

1 6. For use with an operational circuit comprising at least
2 one high-impedance node, a pull-up circuit capable of pulling said
3 high-impedance node up to a high voltage when a pull-up (PU*)
4 signal driving said pull-up circuit is Logic 0, said pull-up
5 circuit comprising:

6 a first pull-up P-channel transistor having a drain
7 coupled to said high-impedance node, a gate coupled to said PU*
8 signal, and a source coupled to a common node;

9 a second pull-up P-channel transistor having a drain
10 coupled to said common node, a gate coupled to said PU* signal, and
11 a source coupled to a VDD power supply rail, wherein said first and
12 second pull-up P-channel transistors are off when said PU* signal
13 is Logic 1 and are on when said PU* signal is Logic 0; and

14 a gate-biasing circuit driven by said PU* signal, wherein
15 said gate-biasing circuit is off when said PU* signal is Logic 0
16 and said gate-biasing circuit applies a Logic 0 bias voltage to
17 said common node when said PU* signal is Logic 1, said Logic 0 bias
18 voltage creating a positive Vgs bias on said first pull-up P-
19 channel transistor when said PU* signal is Logic 1.

1 7. The pull-up circuit as set forth in Claim 6 wherein said
2 gate-biasing circuit comprises a biasing N-channel transistor
3 having a gate coupled to said PU* signal, a drain coupled to said
4 common node, and a source coupled to a ground power rail.

1 8. The pull-up circuit as set forth in Claim 7 wherein said
2 operational circuit is a phase-locked loop (PLL).

1 9. The pull-up circuit as set forth in Claim 6 wherein said
2 gate-biasing circuit comprises:

3 an inverter having an input coupled to said PU* signal;
4 and

5 a biasing P-channel transistor having a gate coupled to
6 an output of said inverter, a source coupled to said common node,
7 and a drain coupled to a ground power rail.

1 10. The pull-up device as set forth in Claim 9 wherein said
2 operational circuit is a phase-locked loop (PLL).